Architecture of a Multi-slot Main Memory System for 3.2 Gbps Operation

Jaejun Lee, Sungho Lee, Joontae Park and Sangwook Nam
School of Electrical Engineering and Computer Science
INMC, Seoul National University
Seoul, Korea
jaejun@ael.snu.ac.kr

Abstract—**This paper produces new architecture for a high-data rate and high-density main memory system with bidirectional single-ended signaling. An SSTL-II-based structure has been traditionally been used for chip-to-chip interconnections requiring high-speed and high-density for the main memory system. However, this structure is no longer applicable for a high-speed memory system with high-density. By finding an optimum reflection coefficient at the slot position and determining the transmission line impedance, a multi-slot system can be made to act like a point-to-point system. The proposed main memory system shows significantly improved the signal integrity. The simulated jitter and eye openings, including transmission line loss, were improved by 69.9% for writing and 63.0% for reading at 3.2 Gbps.**

I. INTRODUCTION

Over the last decade, the performance of processors and processing system including personal computer (PC) systems has been improving at an accelerated rate. In particular, the main memory systems have increased dramatically with larger bandwidth and higher density. And the ongoing demand for faster speed and higher capacity of the memory system. Currently, reliable communication between the memory controller and dynamic random access memory (DRAM) is a major challenge in this field, due to the high operation frequency and several module effects from the number of dual inline memory modules (DIMMs) attached to the memory channel. Multi-drop buses with a number of slots have traditionally been used for the main memory buses in PCs, including the current DDR3 main memory system, to satisfy the high density and high frequency. However, as the data rates on these buses have increased, the maximum number of slots per channel has been reduced in order to maintain the signal integrity. That is, the number of slots per channel has been reduced due to intersymbol interference (ISI) caused by signal reflections at impedance mismatches in multi-drop bus junctions and terminations. Although the capacity per memory module is increased, the reduction in memory slots per memory channel limits the memory capacity per memory channel [1]. For these reasons, DDR3 main memory buses have been restricted to only two slots per channel. In the near future, the point-to-point bus type by which a driver and receiver communicate via a one-on-one interconnection will prevail for main memory bus types such as graphic DDR (GDDR) memory systems as long as the DRAM has no equalizer circuits. As another example, techniques such as parallel channels and fully buffered DIMM (FBDIMM) [1] are used to fulfill memory capacity and speed demands, but these are high-cost system in terms of input/output pins, PC board area, extra error correction circuits, and thermal issues.

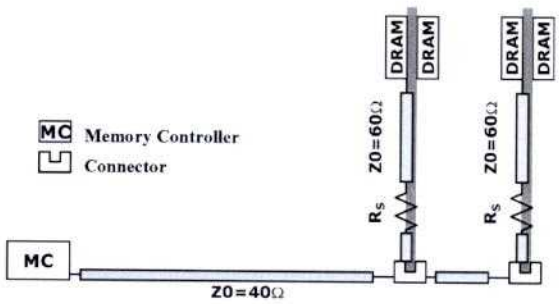

Figure 1. DDR2 and DDR3 main memory bus system

TABLE I. ODT CONFIGURATION FOR DDR3 TWO-SLOT MAIN MEMORY ARCHITECTURE

Operation Status	ODT Values (Ω)		
	MCH	*1st Slot*	*2nd Slot*
Write to 1st Slot	x	60	20
Write to 2nd Slot	x	20	60
Read from 1st Slot	50	x	20
Read from 2nd Slot	50	20	x

* All DIMMs are double ranks [4]

Numerous papers have been published on equalizer circuits used to eliminate distortion at the receiver block, such as the feed forward equalizer and the decision feedback

978-1-4244-5309-2/10/$26.00 ©2010 IEEE

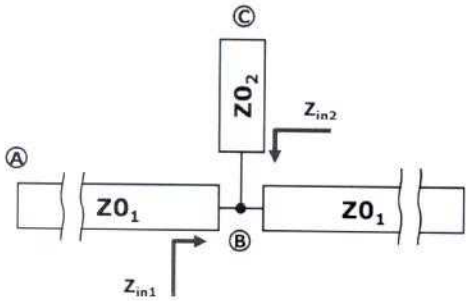

Figure 2. The basic topology of multi-slot main memory system

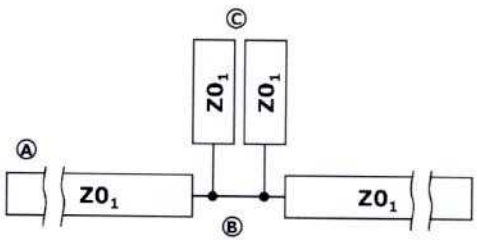

Figure 3. Example of the equivalent topology to the concept of the proposed topology

equalizer [2]. While these equalizer schemes have been good solutions for solving the ISI problems in backplanes, they are unsuitable for low-power, low-cost systems like the main memory system with a great deal of reflection noise.

Therefore, this paper introduces a new type of multi-drop bus for the main memory channel, which acts electrically like a point-to-point bus. The proposed multi-drop bus scheme improves the signal integrity at the higher operating frequency, reducing the total jitter and widening eye openings. In addition, this system reduces the design specification burden of the memory controller and DRAM in the memory module that operates over 3.2 Gbps and does not include an equalizer. This method can be applied to high-speed signaling through a parallel link as well as the main memory channel.

II. Design of Main Memory Channel Architecture

Since the best interconnection between the two chips is point-to-point wiring, the basic concept of the new multi-drop bus topology is minimizing the reflection noises from the channels as in a point-to-point bus topology. The conventional multi-drop bus topologies used in DRAM channels for DDR2 and DDR3 main memory systems are based on SSTL-II, as shown in Figure 1. This SSTL-II based structure has inherent reflection noise, which makes them sufficient for use at the relatively low frequencies. In addition, with the configuration of the on-die-termination (ODT) circuit given in Table I and a low-impedance (40Ω) transmission line on the PC board, the SSTL-II structure can be extended to a 1.6 Gbps operation frequency like the DDR2 and DDR3 memory systems shown in Figure 1.

A. Concept of the Proposed Multi-drop Bus Topology

The conventional DDR2-3 main memory bus topology based on SSTL-II has structural weak points in relation to practical applications. The gaps of between each slot and the length of the junction to the module resistor, R_S, prevent perfect matching at the junctions of the multi-drop point and connectors, as shown in Figure 1. For these reasons, residual reflection noises exist in the channel.

However, as shown in Figure 2, since point C is the end of an open stub, the open-circuit voltage at point C is twice the input voltage. This means that the voltage at point C is the same as that at point A when the voltage at point B is half the initial voltage at point A. To create this special condition, the structure must satisfy that the reflection coefficient Γ_{in1} is equal to $-1/2$ and the input impedance Z_{in1} is Z0/3 by (1) at that time.

$$\Gamma_{in1} = \frac{Z_{in1} - Z0_1}{Z_{in1} + Z0_1} = -\frac{1}{2} \Leftrightarrow Z_{in1} = \frac{Z0_1}{3} \tag{1}$$

From the obtained optimal values Z_{in1}, the optimal impedance $Z0_2$ of the branch can be found by (2).

$$Z_{in1} = Z0_1 // Z0_2 = \frac{Z0_2 \cdot Z0_1}{Z0_2 + Z0_1} \Leftrightarrow Z0_2 = \frac{Z0_1}{2} \tag{2}$$

Thus, the optimal impedance $Z0_2$ is half of $Z0_1$. In addition, the reflected signal at point C of Figure 2 does not come back to the point C again, because Z_{in2} is Z0/2 and Γ_{b2} is zero by (3).

$$\Gamma_{b2} = \frac{Z_{in2} - Z0_2}{Z_{in2} + Z0_2} = 0 \tag{3}$$

From the conceptual bus topology shown in Figure 2, the relationship between the impedance of the branch, $Z0_2$, and the number of the branches, N, follows (4) to only retain the property that the impedance of branches is electrically equal to half the main impedance $Z0_1$.

$$Z0_2 = \frac{Z0_1}{2} \cdot N \tag{4}$$

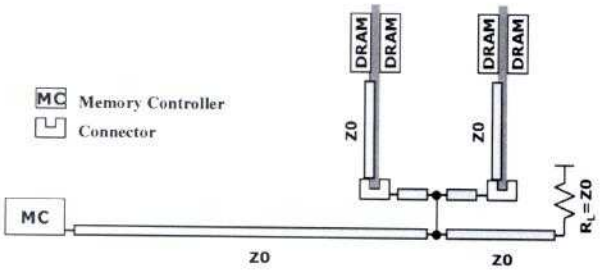

Figure 4. Proposed main memory bus system with two slots

TABLE II. ODT CONFIGURATION FOR THE PROPOSED TWO SLOT MAIN MEMORY ARCHITECTURE

Operation Status	ODT Values (Ω)		
	MCH	*1st Slot*	*2nd Slot*
Write	x	x	x
Read from 1st Slot	75	x	50
Read from 2nd Slot	75	50	x

* Channel Z0 of PC board and DIMM is 50Ω

For example, in the case of a two-drop bus topology, both the main transmission line and the branch trace have the same impedance ($Z0_2 = Z0_1$), by (4), as shown in Figure 3. Furthermore, the topology in Figure 3 is exactly equivalent to that of the proposed conceptual bus topology in Figure 2 in its electrical characteristics. From (4), the proposed structure seems to be applicable for many branches; however, the practically, the maximum number of branches (slots) may be around three or four, and a topology with two branches may be the best choice, considering the impedance of the memory module.

B. Practical Structure of Proposed Main Memory Bus Topology

Figure 2 shows the present DDR3 main memory system architecture. For 1.6 Gbps operation in the memory channel, the maximum number of slots must be restricted to two. This means that this topology cannot be applied over 1.6 Gbps. Therefore, the ultimate solution for operation over 1.6 Gbps is a one-slot memory system which drives the high-speed memory system and relinquishes the high-density system. Moreover, the present DDR3 main memory architecture lacks routing space in the PC board, since 40Ω impedance traces are applied to PC boards to improve the signal integrity for the write operations. An impedance of 40Ω is about twice the width of an impedance of 60Ω. Therefore, this conventional topology occupies more routing area. In addition, all DRAMs require an ODT with a complicated configuration such as that in Table I [4]. Furthermore, different kinds of values of ODT options are needed; this is one of the design burdens that include the die area penalty. Moreover, the current flowing through these ODTs may cause thermal issues.

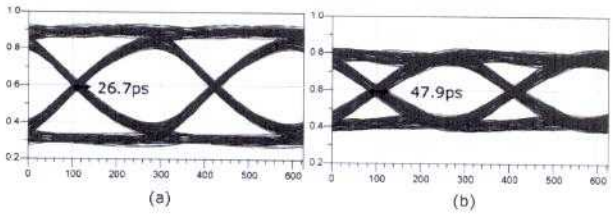

Figure 5. (a) Eye diagram of write operation and (b) eye diagram of read operation for the proposed the architecture in two slot heaving loading case at 3.2Gbps

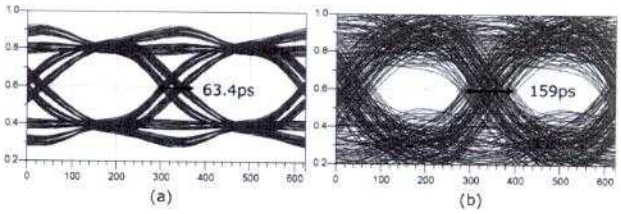

Figure 6. (a) Eye diagram of write operation and (b) eye diagram of read operation for the conventional DDR3 architecture in two slot heaving loading case at 3.2Gbps

TABLE III. COMPARISON OF DDR3 CONVENTIONAL ARCHITECTURE AND PROPOSED ARCHITECTURE IN 3.2GBPS

Operation	WRITE			READ		
Architecture type	P-P Jitter	RMS Jitter	Eye Height	P-P Jitter	RMS Jitter	Eye Height
DDR3	63.4ps	20.3ps	399mV	159ps	31.9ps	240mV
Proposed 2 slot	26.7ps	6.1ps	415mV	47.9ps	11.8ps	290mV

* All DIMMs are double ranks

Figure 4 shows the new architecture of the main memory system comprising the proposed topology given in Figure 3. As shown in Figure 4, the trace impedance of the DIMM is the same as the impedance Z0 of the PC board. This characteristic makes it easy to produce and apply to a multi-drop bus system, which overcomes the routing area for the PC board. In addition, as shown in Table II, the ODT control scheme and values are simplified compared to Table I. Since the current does not flow to the DRAM with the write operation and termination values are higher than before with the read case, thermal issues in the DRAM are reduced. Moreover, in prior topologies as shown in Figure 1, the length of the DIMM tab to the resistor (R_S in Figure 4) and the slot-to-slot length worsen the signal integrity. However, in the proposed DIMM scheme, the trace length of the DIMM is independent, except for attenuation effect. Therefore, these characteristics of the new topology can be extended to over 3.2 Gbps by using a pre-emphasis driver to overcome only the high-frequency attenuation.

The signal integrity of the proposed topology is sensitive to the loading balance between the two slots. A dummy DIMM for which the electrical length and loading conditions

are the same as for a normal DIMM is needed when only one DIMM is populated in the main memory channel. Finally, even though the trace width in the PC board can be reduced in the new topology, the routing density can increase in the slot-to-slot area because a T-branch must exist in the area of the connectors for the proposed structure.

III. Simulation Results

To validate the proposed method, simulations were performed for the two-slot memory system with an FR-4 substrate ($\varepsilon_r = 4.1$), which is generally used in PC boards and DIMMs. The connector model used was the current DDR3 connector model. The Advanced Design System (Agilent Technologies) was used to simulate the signal integrity of the memory system. For the simulation, a VDD of 1.2V and ideal voltage sources with a turn-on resistance were used. The DRAM package model was the same as the DDR3 BGA package model. The length of the memory controller to the first connector was set to 101.6mm and the distance of the two connectors was 12.7 mm. The PC board impedance was 40 Ω, and the impedance for the DIMM was 60 Ω for the present DDR3, whereas the trace impedance of the proposed architecture was 50Ω for both the PC board and DIMM. For the 3.2Gbps operation conditions, eye diagrams were produced for a double rank, two-slot system, as shown in Figures 5 and 6. In both cases of the write and read operations, RMS jitter was improved by 69.9% for writing and 63.0% for reading, as shown in Table III. In addition to the jitter, the eye height was also improved. A significantly reduced jitter improves the timing margin when the memory system reads from DRAM and writes to DRAM.

IV. Conclusion

In this paper, an effective architecture of the main memory system is proposed to minimize reflection noise and be extended to a higher frequency with multiple slots. As a result, the system can obtain better jitter and eye height than the conventional main memory structure based on SSTL-II. In addition, since the current does not flow to the operating DRAM, we look forward to diminishing thermal problems in the present DDR3 memory module. Therefore, the proposed architecture can be used as a high-frequency, high-density solution for the future main memory systems.

Acknowledgment

This work was supported by the Korea Science and Engineering Foundation (KOSEF) through the National Research Lab. Program funded by the Ministry of Education, Science and Technology (No. ROA-2007-000-20118-0 (2007)).

References

[1] J. Haas and P. Vogt, "Fully-buffered DIMM technology moves enterprise platforms to the next level," Technology@Intel Magazine, March 2005.

[2] H. Fredriksson, C. Svensson, "2.6 Gb/s Over a Four-Drop Bus Using an Adaptive 12-Tap DFE," European Solid-State Circuits Conference, pp. 470–473, Sept. 2008.

[3] H. Chung, Y. Jang. *et al.*, "Channel BER Measurement for a 5.8Gb/s/pin Unidirectional Differential I/O for DRAM application," IEEE Asian Solid-State Circuits Conference, pp. 29–32, Nov. 2008.

[4] K. Elissa, "DDR3 SDRAM specification," JEDEC STANDARD, JESD 79-3B, Apr., 2008.

[5] M. S. Sharawi and M.T. Al-Qdah, "The Design and Simulation of a 400/533Mbps DDR-II SDRAM Memory Interconnect Bus," IEEE International Multi-Conference on Systems, Signals and Devices, pp. 1–6, Jul., 2008

[6] W. T. Beyene and A. Amirkhany, "Controlled Intersymbol Interference Design Techniques of Conventional Interconnect Systems for Data Rates Beyond 20 Gbps," IEEE Trans. on Advanced Packaging, Vol. 31, No. 4, pp.731-740, Nov., 2008